We Claim:

1. A packet switching system, comprising:

a plurality of input line processors;

a plurality of input buffers being connected to said input line processors;

each of said input buffers includes a plurality of queue buffers corresponding to said output line processors;

a plurality of output line processors; and

a crossbar switch being connected to said input buffers and said output line processors;

the improvement characterized in that:

arbitration is performed by taking both an interval of time for a packet to be transmitted to the crossbar switch from said queue buffer and a queue length of said queue buffer as parameters, both are calculated for each queue buffer of said queue buffers, to thereby select a queue buffer among all queue buffers in the input buffers and give the selected queue the grant for transmitting a packet to said crossbar switch.

2. A packet switching system as set forth in Claim 1, further comprising:

output data interval measuring means for measuring an interval of time for a packet to be transmitted to the crossbar switch from said queue buffer, and

queue length measuring means for measuring a length of the queue buffer, both measuring each queue buffer of all the queue buffers.

3. A packet processing unit as set forth in Claim 1, wherein the arbitration is performed by taking as a parameter the queue length prior to the time interval so as to prevent packets from overflowing from each of the queue buffers.

4. A packet processing unit as set forth in Claim 1, wherein the arbitration is performed by taking as a parameter the time interval prior to the queue length, so as to shorten a time for a packet to exist in each of the queue buffers.

5. A packet switching system, comprising:

a plurality of input line processors;

a plurality of output line processors;

a plurality of input buffers including a plurality of queue buffers, being provided corresponding to the output line processors, and being connected to the input line processors;

a crossbar switch being connected to the input buffers and the output line processors;

an arbiter to arbitrate for assigning grant of transmitting a packet to said crossbar switch, to any of queue buffers of the queue buffers; and

means to determine priority as a parameter between an interval of time for a packet to be transmitted to the crossbar switch from said queue buffer and a queue length of said queue buffer, both are calculated for each queue buffer of said queue buffers, to thereby select a queue buffer among all queue buffers in the input buffers and give the selected queue the grant for transmitting a packet to said crossbar switch;

wherein said arbiter performs arbitration according to said priority determined on all queue buffers of the input buffers.

6. A packet switching system as set forth in Claim 5, further comprising:

output data interval measuring means for measuring an interval of time for a packet to be transmitted to the crossbar switch from said queue buffer, and

queue length measuring means for measuring a length of the queue buffer, both measuring each queue buffer of all the queue buffers.

7. A packet processing unit as set forth in Claim 5, wherein the arbitration is performed by taking as a parameter the queue length prior to the time interval so as to prevent packets from overflowing from each of the queue buffers.

8. A packet processing unit as set forth in Claim 5, wherein the arbitration is performed by taking as a parameter the time interval prior to the queue length, so as to shorten a time for a packet to exist in each of the queue buffers.